




12/29/00

438	714
Class	Subclass
ISSUE CLASSIFICATION	

PATENT NUMBER

U.S. UTILITY Patent Application

 O.I.P.E. SCANNED  Q.A. 	PATENT DATE
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APPLICATION NO. 09/751979	CONT/PRIOR F	CLASS 438	SUBCLASS 714	ART UNIT 1763	EXAMINER Goudreau
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Akashi Nishizawa

Manufacturing method, semiconductor integrated circuit including simultaneous formation of via hole reaching metal wiring and concave groove in interlayer film and semiconductor integrated circuit manufactured with the manufacturing method

PTO-2040
12/89

ISSUING CLASSIFICATION

ORIGINAL				CROSS REFERENCE(S)								
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)							
438		714		438	725	717	723	724	736	743		
INTERNATIONAL CLASSIFICATION				430	5							
H	0	I	L	21/302	438	751	749	734				

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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. 6	Figs. Drwg. 20	Print Fig. 7C	Total Claims 10	Print Claim for O.G. 1
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED 8-12-03	
	<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____ _____ _____			ISSUE FEE Amount Due Date Paid \$ 1,600	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) (Date)			ISSUE BATCH NUMBER 8/13/03	

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